Uichang Lee et al., Int J Mater Sci Res. 2017
http://dx.doi.org/10.18689/2638-1559.a1.002

Multi-Bit Memory Device with Multi-Layered Ferroelectric Polymer Film

Uichang Lee* and **Woo Young Kim**
Department of Electronic Engineering, Jeju National University, Republic of Korea

Recently, studies on the improvement of the integration degree of memory devices using ferroelectric polymers have been actively conducted. Methods of increasing integration include horizontal physical scaling, storing multiple bits in a single memory cell, and building a stacked structure.

Among them, multi-bit memory is a useful concept to increase the memory capacity with using the existing processes because it can increase the integration degree without reducing the horizontal physical length. In this paper, we point out the problems of the conventional ferroelectric multi - bit memory integration method and propose a multi - bit memory device structure which can improve the degree of integration by using the stacked structure and verify its operation. In addition, the proposed architecture is robust against interference when integrated.

Acknowledgement: This research was financially supported by The Project Management Center Cultivating Smart Grid & Clean Energy Manpowers (CK-1), JNU

Biography:

Mr. Uichang Lee is an undergraduate student at Jeju National University in Korea, and his research interests are semiconductor devices and circuit design. Prof. Dr Woo Young Kim is an assistant professor at Jeju National University in Korea. His research fields include applications of ferroelectric polymer and graphene process.